SECTION XVI

LOW PHASE NOISE OUTPUT (OPTION)

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LOW PHASE NOISE OUTPUT (OPTION)

1 INTRODUCTION

This option is a companion option to one of the following options:

A. Disciplined High Stability 10 MHz Quartz Oscillator option (manual Section XV)
B. Disciplined High Stability 1, 5, 10 MHz Quartz Oscillator (manual Section XV)
C. Disciplined 10 MHz Quartz Oscillator (manual Section XVII)
D. Disciplined High Stability 10 MHz Rubidium Oscillator (manual Section XIV)

1.1 DISTRIBUTION OF LOW PHASE NOISE OUTPUT

This option provides a means of distributing the low phase noise output of the High Stability Quartz Oscillator or the Standard Quartz Oscillator to the user without contaminating it with the digital noise which is present on the power supplies and the backplane bus of the GPS-DC. It provides three isolated 50 ohm signals with substantially the same phase noise and spurious noise characteristics as the oscillator source.

1.2 PHASE LOCKING OF QUARTZ OR RUBIDIUM OSCILLATOR

This option also provides the means of Phase Locking either the (High Stability Quartz Oscillator or the Standard Quartz Oscillator) or (1, 5, 10 MHz High Stability Quartz Oscillator) to the Optional Disciplined Rubidium Oscillator (manual Section XIV). The benefits provided by the phase lock loop are excellent stability and holdover performance of the Rubidium Oscillator with the distributed Low Phase Noise Quartz Oscillator outputs.

This option consists of the 86-357-X (oscillator dependent) Low Phase Noise board.

1.3 DISCIPLINED QUARTZ OSCILLATOR SPECIFICATIONS

Level: 1 Vrms +/- 10% into 50 ohms

Output Z: 50 ohms

Waveform: Sine, Harmonics < -30 dBc

Accuracy: See Section I, Specifications and Section XV, Disciplined High Stability Quartz Oscillator (OPTION)
See Section I, Specifications and Section XVII, Disciplined Quartz Oscillator (OPTION)
See Section I, Specifications and Section XIV, Disciplined Rubidium Oscillator

		High Stability Quartz	Standard Quartz	Rubidium oscillator
SSB Phase Noise:	**f**	**L(f)**	**L(f)**	**L(f)**
	1 Hz	- 90 dBc	- 80 dBc	- 85 dbc
	10 Hz	-120 dBc	-110 dBc	-105 dbc
	100 Hz	-140 dBc	-125 dBc	-130 dbc
	1000 Hz	-145 dBc	-130 dBc	-135 dbc
	10000 Hz	-145 dBc	-130 dBc	-140 dbc
Spurious:	30 Hz < f < 300 Hz	-115 dBc	-100 dBc	-110 dbc
	300 Hz < f < 3000 Hz	-125 dBc	- 90 dBc	-125 dbc
	3000 Hz< f < 25000 Hz	-100 dBc	- 90 dBc	-90 dbc

2 INSTALLATION

This option is factory installed. Field installation is not available for this option.

3 OPERATION

No special operating procedures are required. The low phase noise outputs are accessible from the connectors on the rear panel of the 86-357-X option board.

DAC CONTROL

In this aplication, the clock oscillator, a Disciplined High Stability Quartz, Disciplined Standard Quartz, or Rubidium Oscillator is the source for the Low Phase Noise output distribution. The oscillator signal is routed to the board either by physically being mounted to the board or remotely mounted and routed via coax cable to the board. The oscillator is DAC controlled by the clock for frequency accuracy and thus becomes the reference for the clock and its accuracy (oscilator dependant).

PLL CONTROL

In this application the Low Phase Noise oscillator, a High Stability Quartz or Standard Quartz Oscillator, is the source for the Low Phase Noise output distribution. The oscillator signal is routed to the board either by physically being mounted to the board or remotely mounted and routed via coax cable to the board. The oscillator is Phase Locked to the clocks internal Rubidium, High Stability Oscillator, or external Ref. Input. Frequency accuracy thus becomes the accuracy of the internal / external Ref input.

In the event that the PLL becomes unlocked, the Low Phase Noise oscillator frequency accuracy cannot be determined. For this case, the PLL is monitored for Lock and is fed into the clock FAULT STATUS. The PLL FAULT is a Major alarm condition and STATUS is as follows:

Keypad	Function 72 FAULT STATUS (LPN: OK/UNLOCK)		
Serial	Function 72 FAULT STATUS (LPN: PLL OK/UNLOCKED)		
Front pannel *STATUS LED:		GREEN**	LOCKED
		RED**	UNLOCKED

* Only applicable if part of the top level clock assembly.
** This condition is only applicable if the clock has no other MAJOR or MINOR alarm conditions.

4 THEORY OF OPERATION

After the GPS-DC has warmed up, the 10 MHz or 1, 5, & 10 MHz frequency outputs are available for use. However, frequency accuracy of the outputs cannot be guaranteed until the GPS-DC has tracked satellites for 24 hours.

4.1 POWER SUPPLIES

The 86-357-X option board includes three power supply regulators U21, U10, U9, and U8 operating from the GPS-DC ±12 VDC supplies to provide clean +5 and ±5.1 VDC and +10 VDC power to the low phase noise wide band buffer amplifiers and Phase Lock Loop Circuit.

4.2 LOW PHASE NOISE 10 MHz BUFFERED OUTPUTS

This option is provided as a cleanup and buffer board for the Quartz oscillator. The oscillator, if PC Board mounted is DAC controlled via a 16 bit DAC from the GPS-DC backplane P1-11A. When the oscillator is off board the 10 MHz signal will be routed to the board via coax cable, and the DAC controll will be wired seperatly to the GPS-DC.

Dependent on the Model 86-357-X (oscillator dependent), the 10 MHz signal from the oscillator enters the board at J2, or is coupled to the same location with the optional board mounted Oscillator. The 10 MHz buffered signal passes through a LC filter and on to the rear panel connectors J6, J7, and J8. These are the user accessible low phase noise outputs. Please note that the outputs must be terminated with a 50 ohm load to meet previously described specifications.

4.3 LOW PHASE NOISE 1, 5, 10 MHz BUFFERED OUTPUTS

This option is provided as a cleanup and buffer board for the Quartz oscillator. The oscillator which is PC Board mounted is DAC controlled via a 16 bit DAC from the GPS-DC backplane P1-11A. The 10 MHz signal is buffered and connects to the GPS-DC backplane via P1, pin C3. The board mounted High Stability Oscillator 10 MHz signal enters the board at J2. The filtered 10 MHz signal is buffered and passes through a LC filter and on to the rear panel connector J8.

The 1 and 5 MHz signals from the on board oscillator enter the module at J3 and J4, respectively. The signals are buffered to the output and passes through a 1 and 5 MHz LC filter and on to the rear panel connectors J6 and J7.

The 1, 5, and 10 MHz outputs on the connectors are the user accessible low phase noise outputs. Please note that the outputs must be terminated with a 50 ohm load to meet previously described specifications.

4.4 RUBIDIUM LOW PHASE NOISE 5 MHz, 10 MHz OR 1, 5, 10 MHz PLL CLEANUP OSCILLATOR

The low phase noise Quartz oscillator 10 MHz signal on the 86-357-X board is phase locked to the Optional Disciplined Rubidium Oscillator (manual Section XIV). This option will provide 1, 5, 10, 5 MHz or 10 MHz Low Phase Noise outputs to the rear panel connectors with specifications as listed in the SSB Phase Noise and Spurious chart for the High Stability Quartz Oscillator or the Standard Quartz Oscillator.

The phase lock loop is designed specifically for this Low Phase Noise application. When power is applied, the output of the phase comparator is the sum of both input quantities of the Rubidium and VCO. The phase comparator provides a digital error signal that maintains a 90 degree phase shift between the VCO center frequency and the input signal from the Rubidium. As the oscillators warm up and stabilize, the PLL circuit begins to drive the VCO in the direction which reduces the frequency difference, until phase lock is achieved. When locked, the low frequency filter of the Phase Lock Loop is designed to reject the phase noise of the Rubidium.

If power is momentarily interrupted after phase lock, time to re-lock will depend upon the voltage required to lock the VCO to the Rubidium. Typically this takes less than 10 seconds, but a worst case of 8 minutes to re-lock could be expected after several years of oscillator aging. The outputs of the Cleanup Oscillator are available for use immediately after lock.

4.5 FREQUENCY LEVEL OUTPUT ADJUSTMENTS

The frequency level output level has been set at the factory. If in the event that the oscillator has been changed or the output level has drifted out of spec, this section describes the method for adjustment.

Dependent on the 86-357-X board the adjustment pots will adjust different outputs. Refer to the 86-357 schematic diagram and the 86-357-X assembly drawing and bill of materials to determine which outputs are enabled.

In general, an on-board or off-board oscillator is typically routed into J2 and its output is adjustable via pot R23. For multiple oscillator frequency outputs the signal is routed into J3 and J4 and the outputs are adjustable via pots R33 and R34, respectively.

For applications using the frequency doubler (Ak1 installed), typically a 5 MHz oscillator is doubled to 10 MHz. The 5 MHz output level is adjustable via pot R23 and the 10 MHz level is adjustable via pot R33.

All outputs must be terminated with a 50 ohm load to obtain a 1 VRMS (3 Vp-p) output level.

5 MAINTENANCE AND TROUBLESHOOTING

No maintenance of this option board is required. Due to the specialized equipment and expertise required to measure the phase noise levels of these outputs, there are no user serviceable parts. It is recommended that all repairs be made at the factory.

6 DETAILED DRAWINGS

86-357	UNIVERSAL LPN MODULE	BILL OF MATERIALS / DRAWING